REMARKS

By the present amendment, claims 63 to 71 are pending in the application. Claims 63 and 64 are the independent claims.

Support For Claims

Claim 63

New independent claim 63 is a combination of prior independent claim 1 and prior dependent claim 46.

Claim 64

New independent claim 64 is a combination of prior independent claim 3 and prior dependent claim 47.

Claim 65

New dependent claim 65 corresponds to prior dependent claim 48 or 49.

Claim 66

New dependent claim 66 corresponds to prior dependent claim 50.

Claim 67

New dependent claim 67 corresponds to prior dependent claim 51.

Claim 68

New dependent claim 68 corresponds to prior claim 52.

Claim 69

New dependent claim 69 corresponds to prior dependent claim 54.

Claim 70

New dependent claim 70 corresponds to prior dependent claim 57 or 58.

Claim 71

New dependent claim 71 corresponds to prior dependent claim 59.

§102/§103

Claims 1-3, 10, 17, 22, 23, 46, 47, 51, 52 and 57-62 were rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 5,824,568 to Zechman.

Claims 48-50 were rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 5,824,568 to Zechman in view of U.S. Patent No. 6,441,479 to Ahn.

Claims 53-56 were rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No, 5,824,568 to Zechman in view of U.S. Patent No. 5,232,970 to Solc.

These rejections, as applied to new claims 63 to 71 of the present amendment, are respectfully traversed.

Patentability

The technology disclosed in USP 5,824,568 ("US '568") relates to a process of making an integrated circuit chip composite which coats a wire with conformable dielectric material, and the problems caused by distortion during molding is said to be eliminated. According to the detailed description of US '568, the dielectric material (coating) is important to the success of US '568 in that the wires are coated with the dielectric material after the connection has been made between the conductive side and leads via the wire. This coating must be conformable, the example being a parylene coating. See US '568, Col. 2 starting at line 46. This parylene coating is not a metallic coating or an inorganic coating. Although the Office Action mentions that a metal is included in the coating material for the wire, it is submitted that this interpretation is

a misunderstanding. In US '568, there is no disclosure or suggestion about a coating for the wire that includes a metal. In Fig. 2 of US '568, the wire is coated with parylene coating and further coated with an electrically conductive coating. There is no disclosure or suggestion in US '568 that the wire is directly coated with a metal coating which is a metal comprising one or more of nickel, copper, tin, solder, silver, cobalt, chromium, platinum, palladium and tungsten. There is also no disclosure or suggestion in US '568 of an inorganic material coating for the wire.

It is therefore submitted that independent claims 63 and 64, and all claims dependent thereon, are patentable over U.S. Patent No. 5,824,568 to Zechman.

Although the Office Action takes the position that USP 5,824,568 discloses "the metal layer is aluminum", and USP 6,441,479 discloses "Al and Cu are alternatives and equivalents", (see page 6 of Office Action) it is submitted that this interpretation is a misunderstanding. Claim 2 of USP 5,824,568 defines that an electrical conductive site is "aluminum". Therefore, aluminum is an electrode 3 (electrical conductive site) on a chip. This aluminum is not the coating material.

The technology disclosed in USP 6,441,479 ("US '479") relates to a system-on-a-chip with a multi-layered metallized through-hole interconnection, especially for a chip mounting system and its substrates. Copper and aluminum used in US '479 is as follows. In column 4, lines 55-62, there is description that "In practice, the first ground plane 37a or the powder supply distribution plane 37b is first fabricated by depositing a highly conductive layer, such as copper or aluminum, by simple evaporation, sputtering or electroplating with a typical thickness of about 3 to 5 μm over a first insulating layer 35,

e.g., silicon dioxide, previously deposited over the substrate 17 by, for example, CVD ...". This technology, with a reinforcing material, comprising a metal coating and or an inorganic material coating, is quite different from the present invention. Further, "wiring" is a common usage for the circuit wiring in a semiconductor substrates.

It is therefore submitted that independent claims 63 and 64, and all claims dependent thereon, are patentable over U.S. Patent No. 5,824,568 to Zechman in view of U.S. Patent No. 6,441,479 to Ahn.

Since the secondary reference of U.S. Patent No, 5,232,970 to Solc was only applied to former dependent claims 53-56 and new independent claims 63 and 64 are patentable, there is no need to further discuss U.S. Patent No. 5,232,970 at this time.

Foreign Priority

The present application claims foreign priority under 35 U.S.C. §119 from Japanese Patent Application No. 2000-336520 filed November 2, 2000 and Japanese Patent Application No. 2001-324002 filed October 22, 2001. See Patent Application Transmittal Letter at ¶4. See also Inventors' Declaration.

Certified copies of the priority patent applications were submitted by a paper having a Certificate of Mailing dated July 2, 2002.

Applicants respectfully request to be advised of the status of the claim for foreign priority under 35 U.S.C. §119 and the receipt of the certified copies of the priority documents in the next communication from the Patent and Trademark Office.

CONCLUSION

It is submitted that in view of the present amendment and foregoing remarks, the application is now in condition for allowance. It is therefore respectfully requested that the application, as amended, be allowed and passed for issue.

Respectfully submitted,

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